TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2081 Baishakh

Exam.	**Back**		
Level	BE	**Full Marks**	80
Programme	BEL,BEX, BCT	**Pass Marks**	32
Year / Part	II / I	**Time**	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Convert decimal 39 into Gray code and Excess-3 code. Use 2'S complement method to perform the following addition $(-28+17)_{10}$. [2+2+3]
2. What is the importance of De-Morgan's laws? Show how a two-input XOR gate can be constructed from a two-input NAND gate with required expressions. [2+3]
3. Implement the following function using K-Map.F(A,B,C,D)= $\sum(0,2,4,5,11)+d(3,7,12,15)$. Implement the function using NOR gate only. [4+2]
4. What is a priority encoder? Find out the simplest logic circuit for "e" and "f" segments of the BCD –to-seven segment display decoder. [2+3+3]
5. Design 5×32 line decoder using 3×8 line decodes and necessary logic gates. [5]
6. Design and explain the circuit to add the following bits 1011 and 1100 using block-diagrams. [5]
7. With the help of RS flip-flop, realize JK flip-flop with using excitation table and required expressions. [6]
8. Differentiate between synchronous and asynchronous counter. Design 3-bit synchronous down counter using JK flipflops. [2+6]
9. Describe the operation of 4-bit parallel-in serial-out (PISO) shift register with timing diagram of 1011 data input. [3+3]
10. Design a sequential machine that has a single input 'x' and single output 'y'. The machine is required to 'give high output (y=1) when it detects the serial sequence of x = 1101 message. Use T flip-flops only. [12]
11. Explain the characteristics of CMOS gates and explain logic operation of CMOS 2-input NOR gate circuit with its truth table. [3+5]
12. Describe the operation of frequency counter. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division

2080 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL,BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define Gray Code. Design 3-bit binary to gray code converter circuit with necessary truth table and circuit diagram. [2+3+1]
2. Define positive and negative logic. Realize X-NOR gate using NAND gates only. [2+4]
3. Simplify the Boolean function F (A, B, C, D) = $\sum$ m (0,1,2,4,7,8,9,10,12,15) and don't care condition (5,11,13) using K-Map and implement by only NOR gates. [4+2]
4. Realize the following logic function using a single 1:8 demultiplexer and necessary logic gates. [6]

   Y (A, B, C, D) = $\sum_m$ (0, 2, 3, 5, 7, 8, 10, 13, 15)
5. Design the full-subtractor circuit using decoder and required logic gates. What is a combinational logic circuit? [4+2]
6. Show logic diagram, excitation table and characteristic equation of SR flip-flop. [1+2+3]
7. Explain the operation of 4-bit serial in –serial out shift register with a clear circuit and timing diagram with a positive edge-triggered clock. [4+2]
8. Define a ripple counter. Design an asynchronous mod-11 up-counter with negative edge triggering clock. [2+6]
9. Design a mod-5 synchronous counter using JK flip-flops. [7]
10. Define the propagation delay time. Draw the schematic diagram of a 2-input TTL NAND gate and explain its logic operation. [2+6]
11. Design a sequential machine that has one serial input X and one output Z. The machine is required to give an output Z = 1, when the serial input X contains the message 1010. Use T flip –flop. [10]
12. Sketch the block diagram of the digital frequency counter and describe its operation. [5]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2080 Baishakh

Exam.	Back		
Level	BE	Full Marks	40
Programme	BEL, BEX, BCT	Pass Marks	16
Year / Part	II / I	Time	1 ½ hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Perform the following

   (i) $(1110)_{gray} = (\ )_{BCD}$

   (ii) $(1430)_{10} = (\ )_{excess\text{-}3}$

   (iii) Use 2'S complement method to perform the addition (-28 +17). [2+2+4]

2. State and prove De-Morgan's theorems with necessary diagrams. Realise Ex-OR Gate using NAND Gate only. [5+3]

3. Realize Full Adder Circuit using a 2×4 decoder and using logic gates. [8]

4. Draw the simplest logic circuit for "a" segment of the BCD-to – seven segment display decoder and realize the simplest logic expression using only NOR gates. [4+3]

5. What is the Setup time and hold time of a flip-flop? With the help of excitation table and K-map, convert SR flip-flop into JK flip- flop. [2+6]

6. Explain the operation of 4 bit serial in serial out (SIPO) register with timing diagrams for the given data pattern 1010. [7]

7. Design mod-5 Gray code synchronous up-counter with negative edge triggering clock system. (Use JK flip-flops). [8]

8. Draw and explain the schematic diagram of TTL NOR gate and explain about CMOS characteristics. [4+3]

9. Explain the operation of frequency counter with the help of a block diagram. [6]

10. Design a sequential machine, that has one bit serial input (X) and one output (Z). The machine is required to give an output Z = 1, when the input contains the message 1011. Design the machine using T flip flop. [13]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2079 Baishakh

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic (*EX 502*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define Digital and analog Signal, Explain Gray and Excess 3 code with example. [6]
2. Define positive and negative logic and prove that positive X-OR is equivalent to negative X-NOR. [6]
3. Simplify the function using K-map $F=\sum(1,2,3,8,9,10,11,14)$ and $D = \sum(0,4,12)$. Also realize the simplified circuit using NAND Gates. [3+3]
4. a) Design the logic circuit for 4:2 Priority Encoder. [6]
   b) Design 8:1 Multiplexer using 4:1 Multiplexer and 2:1 Multiplexer. [6]
5. Differentiate between combinational and sequential circuits. Explain the operation of asynchronous mod-12 counter with timing diagrams. [2+4]
6. Explain the operation of 4 bit serial in parallel out (SIPO) register with timing diagram. [4]
7. Convert D flip-flop into JK flip-flop and JK flip-flop into D flip-flop. [4+2]
8. Define Synchronous and Asynchronous counter. Design a MOD-10 synchronous counter and draw its timing diagram. [2+6]
9. Define CMOS parameters shortly and explain logic operation of CMOS 2-input NAND gate circuit with its truth table. [3+5]
10. Design a sequential machine that has a single input 'x' and single output 'z'. The machine is required to give high output when it detects the serial sequence of 001 message. Use JK flip-flops only. [12]
11. With the help of block diagram explain the operation of time measurement circuit. [6]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2079 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What is a Gray code? How is it different than binary code? Convert $(10110)_2$ to Gray code? [2+2+2]
2. State and prove De-Morgan's theorems with necessary diagrams and prove that positive NAND equivalent is equal to negative NOR. [2+4]
3. Simplify the following Boolean function using K-map and draw the circuit of simplified expression using NOR gates only. [6]

   $F = \Sigma m (7, 9, 12, 13, 14, 15) + \text{don't care } (0, 2, 3, 5)$.
4. Implementations the following Boolean function using a single 8:1 multiplexer. $F(A, B, C, D) = \Sigma m (2, 4, 5, 7, 10, 14)$. [5]
5. Realize a full-substractor logic circuit using a single 1:4 demultiplexer and necessary logic gates. [5]
6. How do you eliminate the switch contacts bounds circuits? Explain the operation of negative edge triggered RS flip-flop along with excitation table. [3+5]
7. Explain the working function of PISO register with timing diagram of 1010 data input. [6]
8. What is an asynchronous counter? Design a synchronous counter with counting sequence: 000, 001, 011, 111, 110, 100, 000, ... using JK flip-flop. [3+6]
9. Modify SR flip-flop into JK flip-flop by helping corresponding excitation table. [6]
10. Design a sequential machine that has one serial input X and output Z. The machine is required to have an output Z = 1 when the input X contains the serial message 1010. [12]
11. Explain the operation of three input TTL NAND gate. What is the significance of totem-pole output in it? [6]
12. How does a multiplexing display function? Explain with necessary diagrams. [5]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2078 Kartik

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) Explain Excess-3 code with suitable examples. [3]
   b) Perform the following code conversions: [2+2+2]
   (i) $(41.8125)_{10} = (?)_2$
   (ii) $(1000)_2 = (?)_{BCD}$
   (iii) $(19)_{10} = (?)_{Ex\text{-}3code}$
2. Realize full adder circuit using decoder and gates. Subtract $(43)_{10}$ from $(57)_{10}$ using 2's complement method. [3+3]
3. Realize a following logic expression using a 4:1 multiplexer and standard logic gates.
   $Y(A, B, C) = \prod M(0, 2, 6, 7)$ [6]
4. What is a priority encoder? Design an octal priority encoder. [2+6]
5. Show logic diagram, characteristics table of JK Flip flop and derive its characteristics equation and excitation table. [7]
6. Draw the circuit diagram of Serial In Serial Out and Serial In Parallel Out shift register and explain one of them. [3+4]
7. Construct asynchronous T flip-flopped mod-12 up-counter and use positive edge triggered clock. [7]
8. A sequential machine which has one input, A and one output, Y. The machine is required to give the output high when the input contains a serial message of 1001, use only D flip-flops for realizing the design. [12]
9. a) Draw the CMOS logic level profile for both input and output. [3]
   b) Explain the operation of a CMOS inverter with a circuit diagram. [4]
10. What is a method of multiplexing display? Explain with suitable diagrams. [5]
11. Explain TTL NOR gate with circuit diagram and truth table. What is a propagation delay? [4+2]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2078 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What is BCD code? List the advantages and disadvantages of BCD code. [1+3]
2. State and prove De-Morgan's theorems with necessary diagrams. Construct XOR gate using minimum number of NAND gates. [2+4]
3. Obtain the minimal SOP form of $F(A, B, C, D) = \sum m(3, 4, 6, 8, 10, 15) + d(0, 2, 7, 14)$ using K-map and implement the simplified result using NOR gate only. [3+3]
4. Design a circuit that compares two 2-bit numbers, A and B, to check if they are equal. The circuit has one output x, so that $x = 1$ if $A = B$ and $x = 0$ is $A \neq B$. [5]
5. Design full adder circuit using a 2×4 decoder and gates. [4]
6. Design a 5x32 line decoder using 3x8 line decoder and necessary logic gates. [5]
7. Explain the operation of 4 bit serial in serial out (SISO) register with timing diagram of 1011 data input. [3+3]
8. Explain the operation of positive edge trigger S-R flip-flop with excitation table. Also derive its characteristic equation and state diagram. [3+2+2]
9. Define synchronous sequential circuits. Explain the operation of asynchronous decade counter with timing diagrams and circuit diagram. [1+6]
10. Define parallel counter. Design a mod-6 synchronous up counter using JK flip flop. [1+7]
11. Explain the characteristics of CMOS logic families. Draw the schematic diagram of TTL 2-input AND gate and explain with necessary diagrams. [3+4]
12. Design a sequential machine that has one serial input X and one output Z. The machine is required to give an output $z = 1$ when the input X contains the message 1001. Use S-R flip-flop. [10]
13. With the help of block diagram explain the operation of frequency counter circuit. [5]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL,BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain Gray code with suitable examples. [3]
2. State and prove the De-margin's theorem and perform the addition (-47+27) by using 2' complement method. [3+3]
3. Simplify the function using K-map $F=\Sigma (1,2,3,8,9,10,11,14)$ and $D = \Sigma (0,4,12)$. Also realize the simplified circuit using NAND Gates. [4+2]
4. Describe the importance of parity bits in communication system. Explain 3 bits even parity generator circuit clearly. [2+4]
5. Realize a full subtractor circuit by combining only one 1:4 demultiplexer and standard gates. [5]
6. Explain the operation of 8:1 multiplexer with necessary diagrams. Construct 32:1 MUX using only 8:1 MUXs. [3+3]
7. Explain the serial in parallel-out (SIPO) shift register with timing diagram of 1101 data input. [6]
8. Explain the operation of edge triggered J-K Flip-Flop with necessary diagram and excitation table. [6]
9. Differentiate between combinational and sequential logic circuits. Construct and explain mod-12 asynchronous down counter with negative edge clock triggering system. Use JK flip-flops and necessary logic gates. [2+6]
10. Design the synchronous decade counter using T flip-flop and also show its timing diagram. [8]
11. Explain the operation of TTL two input OR gate with schematic diagram and also define the propagation delay time and power dissipation. [4+2]
12. With the help of block diagram, explain the operation of digital frequency counter. [4]
13. Consider a sequential detector that receives binary data stream at its input 'X' and signals when a serial sequence '1011' arrives at the input by making its output'Y' high, otherwise output remains low. Design a sequence detector state machine using positive edge triggered T flip flops. [10]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Ashwin

Exam.	**Back**		
Level	BE	**Full Marks**	80
Programme	BEL, BEX, BCT	**Pass Marks**	32
Year / Part	II / I	**Time**	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) What is a gray code? Compare with binary numbers. [3]
   b) List the advantages of digital signal over analog signal. [3]
2. Describe De' Morgan's laws with examples. Construct XOR gate using only 3-inputs NAND gates. [2+3]
3. What is a decoder? Realize a 2-to-4 line decoder as a full adder circuit. [1+5]
4. Simplify the following function using K-map. And also draw reduced circuit using NOR gate y(A, B, C, D) = ΠM (0,2,3,8,10,11,12,15) and d=ΠM(7,13,14). [5+2]
5. a) Explain the operation of two 4-bit parallel adder with neat diagram. [5]
   b) Realize the logic circuit of 1×16 DMUX using 1×4 DMUX and gates if necessary. [3]
6. Differentiate between combination and sequential circuit. Explain briefly how latch can be used as bounce eliminator. [2+4]
7. Explain how 1001 data can be stored and retrieve n PISO shift register with neat diagram and truth table. [7]
8. Construct a mod-12 asynchronous up counter with positive clock edge triggering Implement only T flip-flops. [5]
9. Design BCD synchronous counter with circuit diagram, truth table and timing waveform. Use T flip-flop. [7]
10. Draw the schematic diagram of 2-input TTL NAND gate and explain about CMOS characteristics. [4+2]
11. Design a sequential machine with one input x and one output z which gives output z=1 when serial input containts 1011 message. Use J-K flip-flop. [12]
12. With the help of block diagram explain the operation of frequency counter. [5]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Chaitra

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) Explain excess-3 code with suitable examples. [2.5]
   b) Define combinational logic circuit. [2.5]
2. Simplify the function using K-map $F=\Sigma(0,1,4,8,10,11,12)$ and $D=\Sigma(2,3,6,9,15)$. Also convert the result into only NAND gates. [6]
3. Design the operation of octal priority encoder with neat diagram. [7]
4. Design a simplest logic circuit for 'b' segment of the BCD-to-7 segment display decoder. [6]
5. Explain the operation of JK flip flop showing its logic diagram, characteristic table and then derive its characteristic equation and excitation table. [6]
6. Draw a 4 bit PISO shift register and explain its operation along with timing waveform with 1101 data load in input. [6]
7. Explain the working principle of 4 bit down asynchronous counter with neat timing diagram using negative clock edge triggering. [6]
8. Design a mod-6 synchronous counter using T Flip-Flops with timing diagrams. [7]
9. Describe the voltage profile of TTL. Explain the working principle of tristate TTL inverter. [2+6]
10. Design a synchronous sequential machine such that it gives output Z=1 if input contains the sequence of message 011 and it retains in its own state in other condition giving output zero. Use RS-Flip-Flop. [11]
11. Draw the circuit diagram of 3 input CMOS gate and explain its operation. [6]
12. Illustrate time measurement circuit with block diagram. [6]

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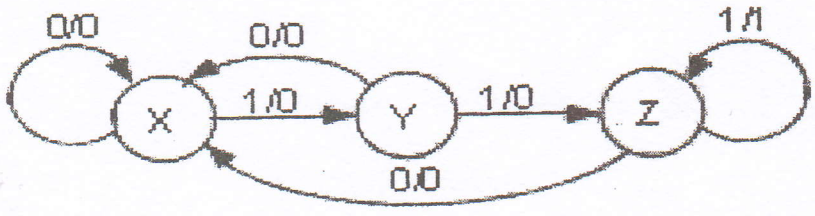
17 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Describe in your own words the characteristics of an analog and a digital signal. Convert A2.64H into its octal and decimal equivalents. [2+4]
2. Explain BCD code with suitable examples. [5]
3. Simplify the function using K-map $F=\sum(0, 1, 4, 8, 10, 11, 12)$ and $D=\sum(2, 3, 6, 9, 15)$. Also realize the simplified circuit using NOR Gates. [4+2]
4. Explain the operation of octal to binary encoder with necessary diagrams. Convert A+B'C in to canonical form. [3+3]
5. Describe the importance of parity bits in communication system. Explain 3 bits odd parity generator circuit clearly. [3+3]
6. Realize the circuit diagram for BCD decoder. Explain 1's and 2's complements with examples? [3+3]
7. Explain the operation of edge triggered S-R Flip-Flop with timing diagram and truth table. [6]
8. Design half subtractor circuit using HDL. [4]
9. Define synchronous sequential circuits. Explain the operation of asynchronous mod-12 counter with necessary diagrams. [1+5]
10. Design a synchronous sequential machine from the state diagram given below. Use S-R Flip-Flop. [10]



11. Explain the operation of 4 bit serial in parallel out (SIPO) register with timing diagram. [4]
12. What is the role of hazards in asynchronous circuit design? Explain two bit magnitude comparator with necessary diagrams. [2+4]
13. Draw the schematic diagram of TTL NAND gate and explain about the transistor switch. [2+3]
14. With the help of block diagram explain the operation of Time measuring circuit. [4]

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17 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2074 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) Define TTL IC Signal levels for Input and Output logic with example. [3]
   b) Convert 37.432 decimal number to binary. [3]
2. a) State and prove De-Morgan's theorems with necessary diagrams. Prove that negative logic OR Gate is equivalent to positive logic AND Gate. [4+2]
   b) What is Gray code? Explain with example. [2]
3. a) Minize the expression and implement the reduced expression by using NAND gates. $F = \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}BCD + \overline{A}BC\overline{D} + A\overline{B}\overline{C}\overline{D} + A\overline{B}C\overline{D} + AB\overline{C}\overline{D} + ABC\overline{D} + ABCD$ [4+2]
   b) What do you mean by Max term? Explain with example. [3]
4. Design the 32:1 Multiplexer using 4:1 multiplexers tree concept and implement the function $F = \sum(0,1,3,8,9,13)$ using suitable Multiplexer. [4+2]
5. a) Explain the operation of 3 bit magnitude comparator with truth table and draw the circuit. [5]
   b) Draw the circuit to add following bits 1011 and 1100. [3]
6. a) Write down the drawback of SR Flip-Flop. Explain the operation of edge triggered JK Flip-Flop with timing diagram and truth table. [2+4]
   b) Explain the operation of 4 bit serial in serial out (SISO) register with timing diagram. [5]
7. Explain the operation of 3 bit Asynchronous up/down counter with timing diagram. [6]
8. Design a synchronous sequential machine such that it gives output Z = 1 if input contains the message 110 and it retains in its own state for other condition giving output zero. Use J-K Flip-Flop. [10]
9. What do you mean by static and dynamic hazards? Give example of static hazards and explain how do you eliminate such hazards? [4+2]
10. With the help of block diagram explain the operation of frequency counter. [4]
11. Draw the schematic diagram of TTL NOR gate and explain about totem pole. [6]

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27 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2074 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) Explain digital wave form based on TTL compatible logic. (Both for input and output) [3]
   b) What is the importance of De-morgan's laws? Show how a two-input NOR gate can be constructed from a two-input NAND gate. [4]
2. Convert decimal 39 into binary and hexadecimal. Use 2'S complement method to perform the following addition (-28+17) [2+3]
3. Simplify the function using K-map $F = \sum(0,1,4,8,10,11,12)$ and $D = \sum(2,3,6,9,15)$. Also realize the simplified logic circuit. [6]
4. a) What is an encoder? Draw the logic circuit of an encoder that converts Octal number into binary. [1+4]
   b) What is a multiplexer tree? Design the 16 to 1 multiplexer using 4 to 1 multiplexer. [1+4]
5. What is the Setup time and hold time of a flip-flop? With the help of excitation table and K-map, convert R-S flip flop into D and J-K flip flops. [2+6]
6. Describe the operation of 4 bit serial in Serial Out shift register, with timing diagram. Consider the input 1011 to be entered into the register. [6]
7. List the advantages and disadvantages of a synchronous counter over asynchronous counter. Design a 3 bit synchronous counter which follow gray code sequence. [2+6]
8. Design a sequential machine that produces output Y = 1 when it detects the serial input X = 100. [10]
9. Define fan-in and fan-out with reference to TTL. With a circuit diagram explain the operation of 2-bit TTL NAND gate. [2+6]
10. Draw the block diagram with decoders to show hour, minute and second. [6]
11. Write short notes on: (any two) [2×3]
    i) Static and dynamic hazzard
    ii) ROM
    iii) DE-MUX tree

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24 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2073 Shrawan

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) Perform the following code conversions. [3+2]
   i) $(1110)_{gray} = (?)_{BCD}$
   ii) $(1430)_{10} = (?)_{Excess-3}$
   b) Construct two input XOR gate using minimum number of 2-input NAND gates only. [5]
2. Implement a full adder circuit using 4:1 Multiplexers. [5]
3. Draw the circuit diagram and explain the working principle of 4-bit parallel in serial out (PISO) shift register. [7]
4. Simplify $\sum 1,2,3,8,10,13 + d(0,4,5,6,7,9,12)$ by using K-Map and write its standard SOP expression. [6]
5. Design 1:32 dimultiplexer tree using 1:8 DEMUXS and 1:2 DEMUXS only. [6]
6. Draw the schematic diagram of TTL Inverter. Explain the working principle of circuit. [3+4]
7. Derive characteristic equation of a JK flip flop. How do you make it a toggle flip flop? Draw the input and output wave form of JK flip flop. [3+2+2]
8. Differentiate between combinational and sequential circuits. Explain BCD-to-Decimal decoder circuit with suitable diagram. [2+6]
9. Design a synchronous MOD-5 counter along with block diagram and timing diagrams. Also write the applications of counters and shift registers. [6]
10. Sketch block diagram of digital frequency counter and describe its operation. [8]
11. A sequential machine has to detect serial input sequance of 101, the machine output will be high. The machine contains two JK flip flops, A and B. Assume: single input, x and single output Y. [12]

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27 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2072 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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- ✓ *Assume suitable data if necessary.*

1. Perform the following as indicated in the brackets: [2×4]
   a. $(10.0101)_2 = (?)_{16}$
   b. $(101001001)_{binary} = (?)_{Gray}$
   c. $(93)_{10} = (?)_{Excess\text{-}3}$
   d. $(10.001)_2 - (11.101)_2$ using ***2's complement method.***
2. a) Describe commutative and associative laws of Boolean algebra with examples and simplify A+A'B=A+B. [2+2]
   b) Implement Excusive OR gate by using NAND gates only. [4]
3. Simplify $\sum 1,2,3,8,9,10,11,13,14 + d(0,4,7,12)$ by using K-Map and write its standard product of sum (POS) expression. [4+3]
4. How do you design 32:1 Mux by using multiplexer tree? Implement logic function $Y = \sum m(0,1,3,8,9,13,15)$ by using suitable multiplexer. [4+3]
5. Realize a full-subtractor using suitable demultiplexer and standard getes. [6]
6. Design a simplest logic circuit for 'b' segment of the BCD to 7 segment decoder. [7]
7. Design and draw the circuit diagram of a 3 bit gray code synchronous counter. [7]
8. Draw ripple decade counter and sketch its timing diagram. [5+2]
9. Draw 2-input TTL NAND gate and explain its working principle. [5]
10. How does second section of a digital clock work? Explain its working principle using block diagram. [6]
11. Design a sequential machine that has a single input 'x' and single output 'z'. The machine is required to give high output when it detects the serial sequence of 011 message. Use JK flip-flops only. [12]

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24RE TRIBHUVAN UNIVERSITY

INSTITUTE OF ENGINEERING

Examination Control Division

2070 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL,BEX,BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define digital signal and explain Gray code with example. [1+5]
2. Prove that positive X-OR is equivalent to negative X-NOR. [5]
3. a) Convert the following term into standard min term. A+B'C. [3]
   b) Use K-map method to implement the following function and also draw the reduced circuit using NOR gate. [5]

   $F(A, B, C, D) = \Sigma_m (0, 2, 4, 6, 8, 10, 15)$ and

   $d = \Sigma_m (3, 11, 14)$
4. a) Realize the logic circuit of the following using 8:1 MUX. [4]

   $F(W, X, Y, Z) = \Sigma_m (1, 2, 5, 7, 8, 10, 12, 13, 15)$

   b) When FF_H is ANDed with CO_H what will be the resulting number? Subtract (26) 10 from (16) 10 using 2's complement binary method. [2+2]
5. a) Differentiate between level and Edge triggering? [3]
   b) Explain the operation of two bit magnitude comparator with truth table and circuit diagram. [5]
6. a) Describe different types of registers with diagram. [8]
   b) Illustrate how 1011 data can be stored and retrieve in parallel in serial out shift register with neat timing diagram and truth table. [8]
7. Differentiate synchronous and asynchronous sequential circuits. Explain the operation of mod-12 synchronous counter with timing diagram. [2+6]
8. a) Define state diagram and state table with example. [2]
   b) Design a sequential machine that has one serial input and one output z. The machine is required to give an output z = 1 when the input X contains the message 110. [8]
9. Draw the schematic diagram of TTL two input NOR Gate. [6]
10. Explain briefly the block diagram of an instrument to measure frequency. [5]

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25 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2069 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define digital IC signal levels. What is Gray Code? Explain with example. [3+3]
2. Construct the given Boolean function: F = (A+B) (C+D) E using NOR gates only. [4]
3. Simplify F (A,B,C,D) = π (0,2,5,8,10) + d(7,15). Write its standard SOP and implement the simplified circuit using NOR gates only. [4+4]
4. a) What is priority Encoder? Design octal to binary priority encoder. [2+4]
   b) Design a 2 bit magnitude comparator. [4]
5. Design a combinational logic that performs multiplication between two 4 bit numbers using binary parallel adder and other gates. [8]
6. Draw the circuit diagram and explain the operation of positive edge triggered JK flip-flop. What are the drawbacks of JK flip-flop? [7+1]
7. Explain the Serial in Serial out (SISO) shift register with timing diagram. [4]
8. Design the synchronous decade counter and also show the timing diagram. [8]
9. Design a sequential machine that detects three consecutive zeros from an input data stream X by making output, Y = 1. [12]
10. Draw the schematic circuit for CMOS NAND gates. What do you mean by totem-pole output? [4+4]
11. Describe the operation of a frequency counter. [4]

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25 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2068 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. List out the name of universal gates and why they are called universal gate? Relise Ex-OR Gate using only NAND gates. [2+2]
2. Explain Excess 3 code with suitable examples. [6]
3. Simplify the function using K-map F= $\sum(0,1,4,8,10,11,12)$ and D = $\sum(2,3,6,9,15)$. Also convert the result into standard minterm. [3+5]
4. Design a 32 to 1 multiplexer using 16 to 1 and 2 to 1 multiplexers. [5]
5. Design a 3-bit even parity generator and 4-bit even parity checker circuit. [5]
6. Draw the block diagram of n-bit full adder and explain its operation. [8]
7. Write down the drawbacks of SR flip flop. Explain the operation of data flip flop with timing diagram and truth table. [1+7]
8. With clear circuit and timing diagram, explain the operation of Serial in - Serial out shift register. [4]
9. Define ripple counter. Explain the operation of mode-10 ripple counter with timing diagram. [1+7]
10. Design a sequential machine that has one serial input and one output z. The machine is required to give an output z = 1 when the input x contains the message 1010. [12]
11. Describe the voltage profile of TTL. Explain the operation of TTL to CMOS interface. [2+6]
12. What is frequency counter? Explain with block diagram. [4]

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26 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2068 Baishakh

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Draw the general input output voltage profile for TTL gates and also mention the noise margin. What do you mean by Gray code? [3+1+2]
2. Why NAND and NOR gates are called Universal gates? Illustrate with examples. [4]
3. What do you mean by HDL? Design a 2 to 4 line decoder circuit using HDL. [2+3]
4. Simplify $\pi(0, 4, 5, 8, 9, 11, 15)$ using K-Map and write its standard SOP expression. [4+2]
5. Draw the circuit of 4 bit RCA (Ripple Carry Adder), using only block diagrams. What are the problems associated with RCA. Explain how these problems can be eliminated. [4+2+2]
6. Draw the schematic diagram of TTL NOR gate. Discuss the characteristics of TTL 74XX series gates. [6]
7. Draw the circuit diagram of edge triggred JK flip flop and explain it. [5]
8. What is a shift register? With clear timing diagram, describe the operation of a 4-bit parallel - in serial - out (PISO) shift register. [2+6]
9. What is a counter? Design a MOD - 6 synchronous counter. Draw its timing diagram.
10. Design a synchronous state machine with the following specification: [12]
    a) No. of input:1
    b) No. of output:1
    c) The output of the machine is to be set high when the data in the input is 110 in sequence, starting from the MSB (Use SR flip - flop).
11. With an example, state and explain the problems associated in the design of asynchronous sequential circuit. [6]
12. Design a two bit magnitude comparator. [6]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Chaitra

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) Explain excess-3 code with suitable examples. [2.5]
   b) Define combinational logic circuit. [2.5]
2. Simplify the function using K-map $F=\sum(0,1,4,8,10,11,12)$ and $D=\sum(2,3,6,9,15)$. Also convert the result into only NAND gates. [6]
3. Design the operation of octal priority encoder with neat diagram. [7]
4. Design a simplest logic circuit for 'b' segment of the BCD-to-7 segment display decoder. [6]
5. Explain the operation of JK flip flop showing its logic diagram, characteristic table and then derive its characteristic equation and excitation table. [6]
6. Draw a 4 bit PISO shift register and explain its operation along with timing waveform with 1101 data load in input. [6]
7. Explain the working principle of 4 bit down asynchronous counter with neat timing diagram using negative clock edge triggering. [6]
8. Design a mod-6 synchronous counter using T Flip-Flops with timing diagrams. [7]
9. Describe the voltage profile of TTL. Explain the working principle of tristate TTL inverter. [2+6]
10. Design a synchronous sequential machine such that it gives output Z=1 if input contains the sequence of message 011 and it retains in its own state in other condition giving output zero. Use RS-Flip-Flop. [11]
11. Draw the circuit diagram of 3 input CMOS gate and explain its operation. [6]
12. Illustrate time measurement circuit with block diagram. [6]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Ashwin

Exam.	**Back**		
Level	BE	**Full Marks**	80
Programme	BEL, BEX, BCT	**Pass Marks**	32
Year / Part	II / I	**Time**	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) What is a gray code? Compare with binary numbers. [3]
   b) List the advantages of digital signal over analog signal. [3]
2. Describe De' Morgan's laws with examples. Construct XOR gate using only 3-inputs NAND gates. [2+3]
3. What is a decoder? Realize a 2-to-4 line decoder as a full adder circuit. [1+5]
4. Simplify the following function using K-map. And also draw reduced circuit using NOR gate y(A, B, C, D) = ΠM (0,2,3,8,10,11,12,15) and d=ΠM(7,13,14). [5+2]
5. a) Explain the operation of two 4-bit parallel adder with neat diagram. [5]
   b) Realize the logic circuit of 1×16 DMUX using 1×4 DMUX and gates if necessary. [3]
6. Differentiate between combination and sequential circuit. Explain briefly how latch can be used as bounce eliminator. [2+4]
7. Explain how 1001 data can be stored and retrieve n PISO shift register with neat diagram and truth table. [7]
8. Construct a mod-12 asynchronous up counter with positive clock edge triggering Implement only T flip-flops. [5]
9. Design BCD synchronous counter with circuit diagram, truth table and timing waveform. Use T flip-flop. [7]
10. Draw the schematic diagram of 2-input TTL NAND gate and explain about CMOS characteristics. [4+2]
11. Design a sequential machine with one input x and one output z which gives output z=1 when serial input containts 1011 message. Use J-K flip-flop. [12]
12. With the help of block diagram explain the operation of frequency counter. [5]

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